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**Poseidon Design**

Poseidon Design Systems was founded in July 2002 to provide system design solutions for companies creating complex SoC solutions using ASIC and FPGA technologies. To date, Poseidon has raised $4 million from the founders, friends and family. During Q1'06, at which time the company expects to be generating revenue, Poseidon plans to seek additional funding in the range of $5M to $10M. Breakeven will occur in 2006 if the company does not raise a VC round, otherwise breakeven is anticipated in 2007. The company has 45 employees.

Today's SoCs typically consist of multiple processor cores, and complex hardware and software design. Engineers must co-design, co-verify and co-simulate both hardware and software, which creates new challenges in system design, and requires a new kind of design tool. To deal with this complexity, a new level of abstraction is required. Behavioral abstraction, often referred to as Electronic System Level (ESL) design, takes the traditional Register-Transfer Level (RTL) design methodology to a higher level.

Using a SystemC simulation environment of the processor and peripherals, the interaction between critical software and hardware subsystems can be optimized, which typically improves the power and performance of a complex system by orders of magnitude, and enables a successful design solution to be reached much more rapidly.

Poseidon offers an ESL tool suite – Triton Tuner and Triton Builder – that automates the process of optimizing and accelerating processor-based designs. Based on a SystemC software and hardware co-simulation environment, transactional-level modeling (TLM) technology, and Poseidon's HW/SW partitioning technology, the Triton tool suite enables SoC designers to co-simulate hardware and software at the architectural level, then tune and accelerate the embedded system for optimal performance, power and cost.

Triton Tuner is a simulation and analysis environment based on SystemC that analyzes the performance of an embedded system, including software performance (using performance counters, code profiling, and bottleneck analysis) and hardware performance (checking memory bandwidth, pipeline stalls, and cache miss-hits). It helps designers

fine-tune a system architecture by determining the optimal HW/SW partition for a given end-use application, and by generating more efficient code based on the new partition.

Triton Builder is a synthesis tool that automatically generates algorithm-specific hardware accelerator blocks in RTL. These new blocks offload the math-intensive algorithms from the host processor, as determined by Tuner's partitioning. Besides accelerating the processing performance for a given algorithm, Builder creates highly efficient communication interfaces to get the data into and out of the custom accelerator hardware.

Poseidon's tools co-simulate the hardware and software at various abstraction levels, including clock-accurate level, and identify the software and hardware bottlenecks for optimizing the system for the best performance. With these tools, engineers can quickly perform design exploration, hardware/software partitioning, and system optimization.

To demonstrate the degree to which the Triton tool suite can accelerate a system, Poseidon has implemented a wavelet encoder for a JPEG 2000 application. Beginning with a design available from the public domain, Poseidon used Triton Tuner to determine the number of execution cycles needed to process a given image – 81.13 million cycles.

By performing an analysis of the system with Tuner, Poseidon identified where and how to optimize the code. The Triton Builder tool was used to partition the design, to generate RTL code for the selected hardware accelerator blocks, and to automatically generate the necessary drivers, test benches and transactional models.

Finally, using Tuner once again, Poseidon performed functional and performance verification before implementing the accelerated design on a Xilinx Virtex-II FPGA. The design employs a MicroBlaze processor supported by instruction and data cache, several peripheral cores, and DDR-DRAM for main memory. The total optimization and acceleration enabled Poseidon to achieve a 23X reduction in execution cycles or 3.54 million cycles.

Poseidon tools support ARM, PowerPC, MicroBlaze and Nios II architectures on ASIC, FPGA and structured array platforms. At the recent GSPx2005 embedded solutions event, Poseidon's Virtex-4 PowerPC accelerator was selected as the best new product in the areas of signal processing, DSPs, embedded applications and EDA tools for developing signal-processing chips or subsystems.

The Triton Builder tool provides designers with the capability to make architecture tradeoffs between the PowerPC APU and PLB interfaces. The APU controller provides a flexible high bandwidth interface between the reconfigurable logic in an FPGA fabric and the instruction pipeline of the integrated IBM PowerPC 405 CPU. With Triton Builder, designers can select a tightly coupled APU and/or a bus-based DMA architecture maximizing the performance of the system.

The ESL industry as a whole is currently $100-200M with an anticipated growth rate in excess of 35%, bringing the total market size to $1.5B in 2008/09. Poseidon's segment of

the market is embedded designs and the company estimates that there are roughly 18,000 embedded design starts in the FPGA, ASIC and Structured Array markets.

Competitors such as Coware supply a simulation solution but are not focused on embedded or accelerated solutions. Celoxica supplies a C to RTL solution but does not have the high speed system solution or simulation technology. Other potential competitors include Critical Blue and Synfora.

Poseidon argues that it is positioned to capture a significant portion of the signal processing applications within the embedded design space. With Triton Tuner and Builder, Poseidon provides a complete system solution for the analysis, optimization, and acceleration of embedded signal processing solutions enabling designers to create better architectures and reduce time to market. The company also has an extensive list of partners including Altera, LSI Logic, Xilinx, ARM, Synopsys, Synplicity, ModelSim, Denali and HiTech Global.

For ASIC designs, a single one-year, time-based, individual license for Triton Tuner ranges from $30K to $50K. Triton Builder ranges from $70K to $95K. The bundled price for a single one-year, time-based license for the Triton suite ranges from $95K-$140K. A simplified version for FPGA designs is $15K for Triton Tuner, $20K for Triton builder and $31.5K for the bundle. Poseidon will continue to develop technologies to raise the level of automation, addressing newer complex architectures and multi-core processing for system-level designers.

Poseidon is scheduled to complete beta evaluations by the end of December and will have revenue generating customers during Q1’06. The company has engagements in embedded signal processing designs in audio, video, VoIP, imaging, wireless, and security applications.

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