The Triton Tuner is a system level design environment which enables designers to quickly analyze their architecture and modify their system for optimal performance. The tool is optimized for Audio, Video, VoIP, Imaging, wireless, storage and security applications.

Most systems consist of processors, caches, memories, buses, peripherals, function blocks, and software algorithms. It is critical for the architecture to support the efficient flow of data between the blocks to meet the performance requirements of the system. The Triton Tuner environment provides the capabilities critical to the designer for developing a robust and efficient solution. Tuner utilizes a SystemC simulation environment based on transaction level models of the system components. The hardware/software cosimulation enables the tool to collect key system performance measurements. These measurements identify the bottlenecks in the architecture which are limiting performance. Tuner provides a user friendly interface and data visualization browser to greatly increase the efficiency of the design effort. Tuner also performs software profiling as well as the collection of system performance indices. These measurements pinpoint inefficiencies in the design and enable the concurrent optimization of the system architecture and the software. Triton Tuner also models the complete memory hierarchy which includes cache memories, write buffers, busses, RAMs, flash memories, etc. With the key performance and utilization data available for the different components of the memory subsystem, you can quickly configure the memory subsystem to achieve maximum performance with lower power consumption.

### Key Functions of Tuner

- Increase system performance by creating an efficient memory hierarchy
- Optimize system performance to create designs with lower power dissipation
- Tune software algorithms to run faster with less hardware inefficiencies
- Reduce system optimization effort by using an effective and user friendly system analysis environment
- Identify hot spots in algorithms through detailed profiling and reduce power by optimizing critical code
- Identify and eliminate bottlenecks between the hardware and the software
### Features

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<th>Features</th>
<th>Benefits</th>
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<td>Application profile plus memory usage data</td>
<td>Easily tune application code and memory hierarchy</td>
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<td>Extensive cache Performance Indices</td>
<td>Tune cache architecture to algorithm</td>
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<td>Memory performance measurements</td>
<td>Select optimum memories - size, type, speed, and configuration</td>
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<td>Correlation between performance data and source code</td>
<td>Identifies problem areas between the application code and the hardware</td>
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<td>Software profiling and Performance Indices</td>
<td>Speeds system bottleneck identification, software optimization and HW/SW partitioning</td>
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<td>User friendly data presentation and visualization</td>
<td>Reduction of analysis time, faster and more accurate tuning decisions</td>
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<td>Co-verification environment based on transactional models</td>
<td>Fast simulation speeds</td>
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### Easy to Identify and correct memory bottlenecks

Using Triton Tuner, bottlenecks in the system design can be identified, isolated and corrected in an easy and quick manner. This greatly facilitates the task of developing a robust architecture which meets the system performance goals. With the key data presentation and user friendly graphical user interface, the designer saves weeks of effort that it takes to develop and optimize a complex system.

### Memory Models

- **Cache**
  - DRAM
  - EDO DRAM
  - SDRAM

- **Scratch Pad**
  - SRAM
  - Write buffer

- **Mem. Contr.**
  - FPM DRAM
  - BEDO DRAM

### Processors Platforms Supported

- ARM™ MicroBlaze™
- PowerPC™
- Nios II™