

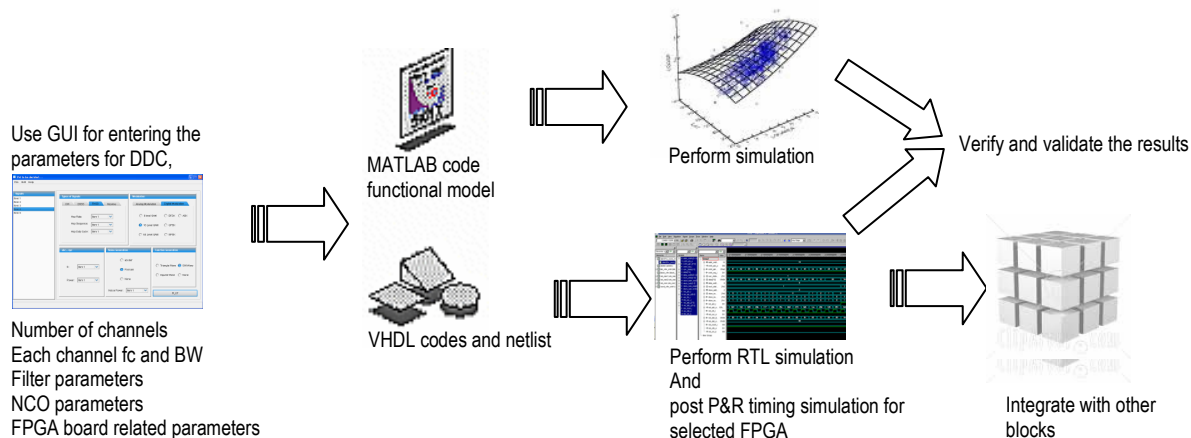
Dynamically configurable DDC core

Release 8.0

Present military and commercial SDR applications the DDC need to switch between different bands of interest. Typical ASIC solutions offer highly programmable DDC channels, but they take several milliseconds of time for switching to a new band. The existing FPGA cores offer hundreds of parallel DDC channels, but occupying major portion of FPGA. Hence the scope of integrating other applications on same FPGA is limited.

Poseidon's Dynamically configurable Digital down converter (DCDDC) core provides DDC core with required number of channels and user can dynamically configure at run time. The GUI front end allows the user to generate the cores for required configuration. As per user requirement either parallel DDC channel based architecture or single DDC with dynamic configuration architecture can be chosen.

To generate the synthesizable cores, user need to give only the required parameters for FPGA settings and required number of channels and bandwidth related information for each channel. A user friendly GUI allows the user to enter all these options. Based on user settings synthesizable VHDL code wrappers and netlist files will be generated. Based on the number of channels chosen the required configuration bits will be generated.



- ◆ Maximum upto 32 channels either in multiplexer architecture
- ◆ User selectable options for CIC and polyphase architecture
- ◆ Dynamically loadable filter coefficients to switch band in less than 1 us time
- ◆ NCO Carrier generation with selected SFDR values (70, 80, 90 and 100 dB)
- ◆ Flexible NCO selection over entire band of operation (with less than 1 Hz resolution)
- ◆ Area optimized DDS based NCO with SFDR more than 90 dB
- ◆ User settable options to choose phase dithering for improving SFDR
- ◆ MATLAB/OCTAVE equivalent codes
- ◆ Modelsim scripts for simulation
- ◆ Flexible licensing options : (a)synthesized netlists and wrapper VHDL(ordering code: SDR-DCDDC-08-SYN)
(b) Full VHDL source code (ordering code: SDR-DCDDC-08-HDL)

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